Design Guide: PMP23338

GaN-based 3.6kW Single Phase Totem Pole Bridgeless PFC with E-meter using C2000™ MCUs.

Description

This reference design is a Gallium nitride (GaN) based, 3.6-kW, single-phase, continuous conduction mode (CCM) totem-pole bridgeless power factor correction (PFC) converter targeting M-CRPS server power supply. This design includes E-meter functionality with 0.5% accuracy using AMCx306 as current sensing device, eliminating the need for external power metering ICs. An alternative low cost current sensing option using TMCS1133 is also provided in this design. The supply is designed to support a maximum input current of 16-ARMS and peak power of 3.6-kW. The power stage is followed by a baby boost converter, which helps to greatly reduce the size of the bulk capacitor. This design can work with either LMG3522EVM-042 or LMG3422EVM-043 GaN EVM. LMG3522R030 and LMG3422R030 are TI 30-mΩ high voltage GaN FET with integrated driver and protections, enable high effciency and high power density. The F28003x C2000™ real-time microcontroller is used for all the advanced controls including re-rush current limit, baby boost operation during AC drop out event, e- metering, and communication between PFC and house-keeping controller. In addition, the F28003x microcontroller has built-in Sigma-Delta filter module to interface with AMC1306 precision current sensing reinforced isolated modulator to achieve industry- leading low total harmonic distortion (iTHD) and high measurement accuracy. The PFC operates at a switching frequency of 65 kHz and achieves a peak efficiency of 98.93%.

Features

- Integrated e-metering function with 0.5% accuracy
- <10% iTHD @ 0-10% load, <5% iTHD @ 10% - 20% load, <3% iTHD @ 20% - 50% load, <2% iTHD @ 50% - 100% load
- Peak efficiency of 98.93% @ 230Vac
- Smart re-rush current control when AC comes back from dropout, meet M-CRPS re-rush current specification
- Include baby boost converter to extend holdup time and allow only 720uF bulk Cap
- Two current sense options: Isolated Delta-Sigma Modulator (default) or Hall Sensor
- GaN optimized with driver integration
- 3.6 kW rated power targeting 73.5 mm M-CRPS PSU.

Resource		Application
PMP23338	Design folder	Rack and server PSU with 48-V output
TMS320F280039	Product Folder	Server PSU with 12-V output
LMG3522R030, AMC1306M05	Product Folder	Server PSU with 12-V output
TMCS1133	Product Folder	Industrial AC-DC
C2000WARE-DIGITALPOWER-SDK	Tool Folder	Single phase online UPS

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WARNING

TI intends this reference design to be operated in a ***lab environment only and does not consider it to be a finished product*** for general consumer use.

TI Intends this reference design to be used only by ***qualified engineers and technicians*** familiar with risks associated with handling high-voltage electrical and mechanical components, systems, and subsystems.

There are ***accessible high voltages present on the board***. The board operates at voltages and currents that may cause shock, fire, or injury if not properly handled or applied. Use the equipment with necessary caution and appropriate safeguards to avoid injuring yourself or damaging property.

CAUTION

Do not leave the design powered when unattended.

High voltage! There are *accessible high voltages present on the board*. Electric shock is possible. The board operates at voltages and currents that may cause shock, fire, or injury if not properly handled. Use the equipment with necessary caution and appropriate safeguards to avoid injuring yourself or damaging property. For safety, use of isolated test equipment with over-voltage and over-current protection is highly recommended.

TI considers it the user's responsibility to confirm that the voltages and isolation requirements are identified and understood before energizing the board or simulation. *When energized, do not touch the design or components connected to the design*.

Hot surface! Contact may cause burns. Do not touch!

Some components may reach high temperatures >55°C when the board is powered on. The user must not touch the board at any point during operation or immediately after operating, as high temperatures may be present.

1. System Description

Bidirectional Totem Pole (TTPL) PFC is an attractive topology for EV chargers and ESS with the trend for higher power, higher efficiency, and higher power density. Table 1.1 describes the bidirectional CCM TTPL PFC reference design power specifications. In this userguide, only PFC operation is described. The inverter mode operation is being developed and will be provided in the subsequent SDK release. Figure 1.1 shows the topology of the implemented PMP23338 reference design. The FET-based relay controls the inrush current. In Figure 1.2, the image of the hardware is shown. Different components of the hardware are described in the following subsections.

Table 1.1. Bidirectional CCM TTPL PFC reference design power specifications.

Parameter	Specification
Input Voltage	85-265V RMS
Input Current	16A RMS maximum
Output Voltage	385V DC bus nominal
Output Current	9.35A maximum
Power Rating	1.8kW : Low Line 3.6kW : High Line
Current THD	<10% iTHD @ 0-10% load, <5% iTHD @ 10% - 20% load, <3% iTHD @ 20% - 50% load, <2% iTHD @ 50% - 100% load
Efficiency	Peak 98.93% at 230V RMS input, Peak 98% at 115V RMS input
Primary Filter Inductor	250uH
Output Capacitance	720uF
PWM Switching Frequency	65kH

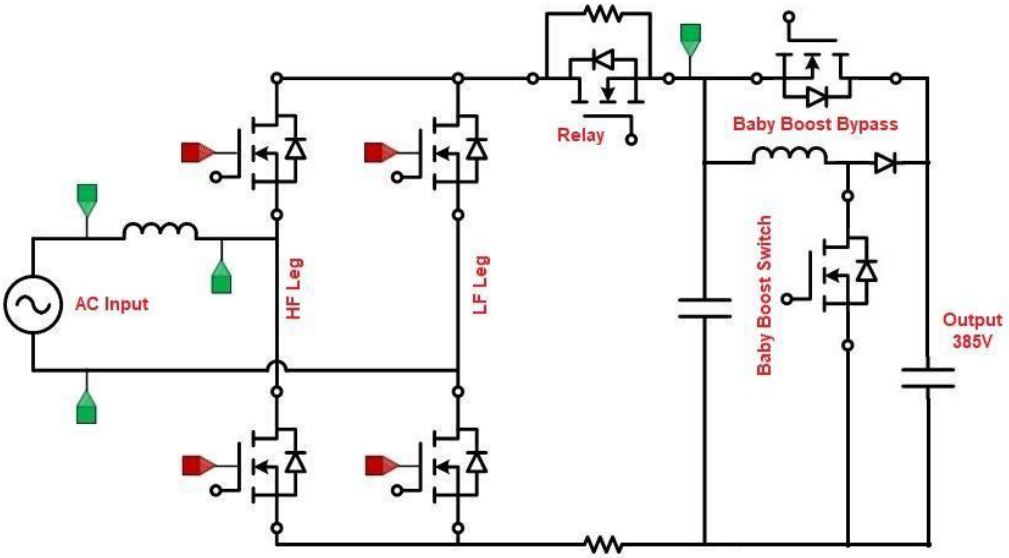


Figure 1.1. Totem pole PFC topology.

Board side view

Board top view

Figure 1.2. Image of PMP23338 main board.

The following gives the detail of the sensing circuit that is on this design

1.1. Input AC voltage sensing

The line and the neutral voltages are sensed by resistor divider to the ground of the board as shown in Figure 1.3. The two readings are subtracted on the controller to get the Vac sensing.

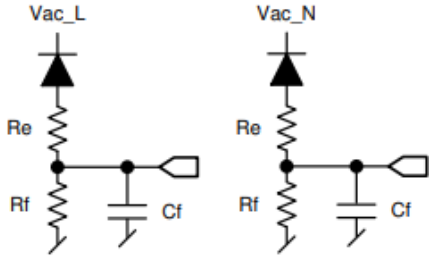


Figure 1.3. Input AC voltage sensing.

1.2. Bus Voltage Sensing

Similarly, the bus voltage is sensed by a resistor divider network as shown in Figure 1.4.

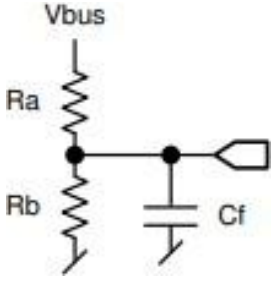


Figure 1.4. Bus voltage sensing.

1.3. AC Current Sensing

This reference design has hall effect and SDFM based current sensing options. One of them can be selected by user by making appropriate change in the code.

1.3.1. Hall Effect Current Sensing

Use a hall effect sensor TMCS1133 to sense input current. This is a conventional current sense method. The output of the hall sensor is amplified by an op-amp circuit (Figure 1.5(a)). With sine wave AC input, the output of hall sensor is a sine wave with a DC offset. This signal is measured by C2000, then subtract the DC offset to get the real AC input current signal.

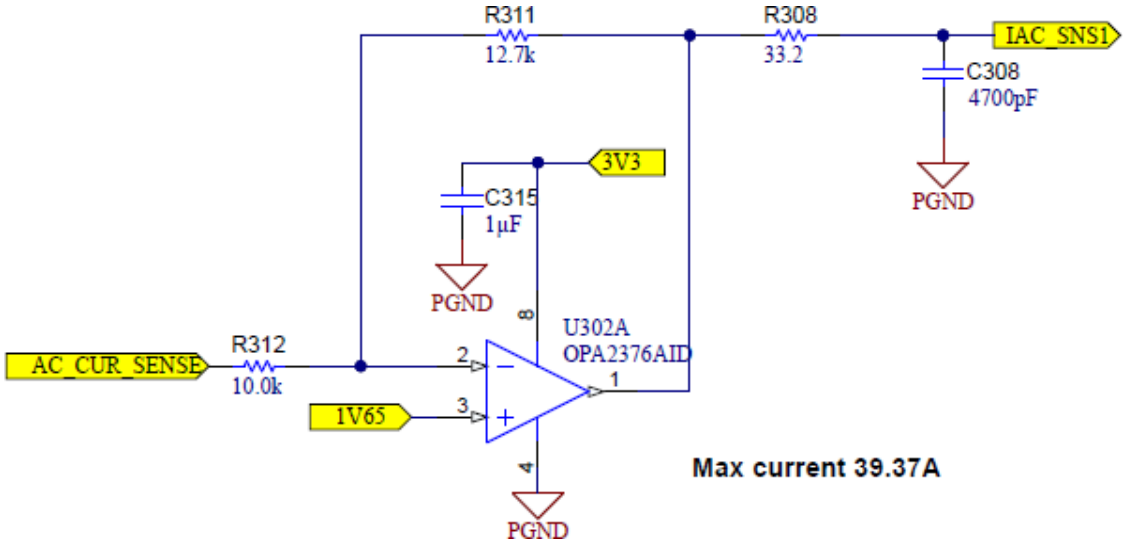


Figure 1.5(a). AC current sensing using Hall effect sensor.

1.3.2. SDFM based Current Sensing

SDFM-based current sensing must be used when E-meter application is needed. The block diagram of the SDFM based AMC1306 is shown in Figure 1.5(b). The analog input at AINP-AINN, which is proportional to the current to be sensed, is digitalized into 1-bit output stream. The isolated data output (Dout) of the converter provides a stream of digital ones and zeros that is synchronous to the externally provided clock source at the CLKIN pin. The Dout signal is filtered using SDFM filter built in F28003x microcontroller. Each SDFM module on F28003x MCU has four SDC and SDD pins where the same Dout signal can be processed differently to achieve different accuracy/conversion speed. In this design, two different filters/pin of a SDFM module are used for the same current sensing. One filter is configured for higher accuracy for E-metering application. The other filter is configured for higher speed for PFC control.

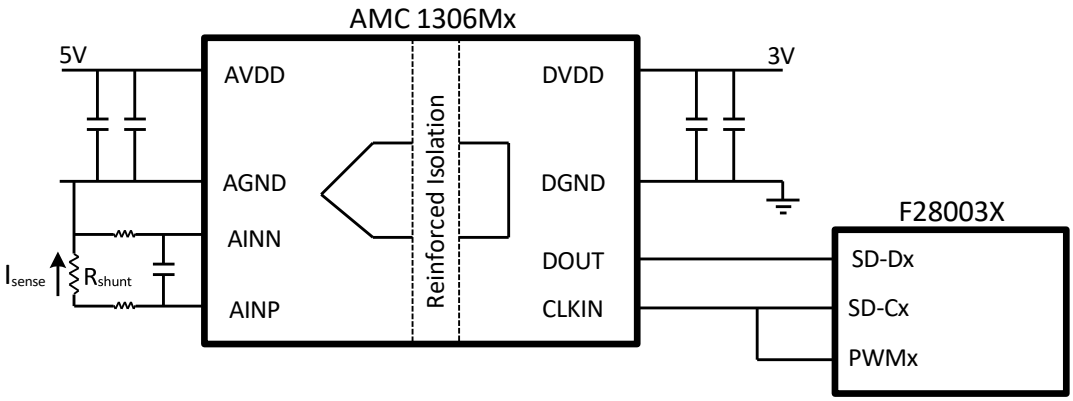


Figure 1.5(b). AC current sensing using SDFM based sensor.

1.4. Sense Filter

An RC filter filters the signals before connecting to the controller. A common RC filter is used for all the sensing signals in this design as shown in Figure 1.6.

Figure 1.6. RC Filter.

1.5 Protection (CMPSS)

Most power electronics converters require protection from overcurrent event. For this design, multiple comparators are required, and references for the trip must be generated, as shown in Figure 1.7.

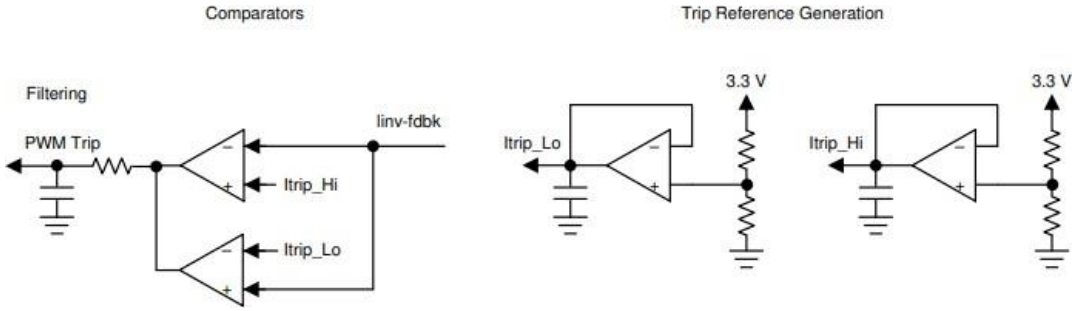


Figure 1.7. Trip Generation for PWM Using Comparators and Reference Generators.

All this circuitry is avoided when using C2000 MCUs, such as TMS320F280039C, which have on-chip windowed comparator as part of the CMPSS that are internally connected to the PWM module that can enable fast tripping of the PWM. An on-chip windowed comparator saves board space and cost in the end application as extra components can be avoided using on-chip resources, as shown in Figure 1.8.

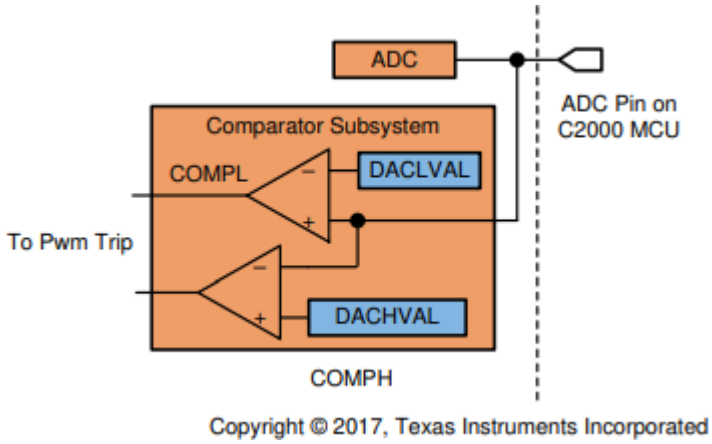


Figure 1.8. CMPSS Used for Overcurrent Protection.

The software has the option to choose either one-shot protection or the cycle-by-cycle (CBC) protection. By default, CBC is selected in the software. To choose one shot protection, comment out `#define TTPLPFC_BOARD_PROTECTION_AC_CUR_CBC_1` in the file “ttplpfc-user_setting.h”.

1.6. Highlighted Products

1.1.1 C2000™ MCU

PMP23338 is implemented using C2000 F28003x control card . C2000 MCUs are part of an optimized MCU family for real-time control application. Fast and high-quality analog-to-digital controller enables accurate measurement of the current and voltage signals, and an integrated comparator subsystem (CMPSS) provides protection for overcurrent and overvoltage without use of any external devices. The optimized CPU core enables fast execution of control loop. Trigonometric operations are accelerated using the on-chip trigonometric math unit (TMU). The solution also provides an option to use the control law accelerator (CLA) on the F28004x and F28003xx. The CLA is a co-processor that can be used to alleviate CPU burden and enable faster-running loops or more functions on the C2000 MCU.

LMG3522R030

The LMG3522R030 single-channel GaN power stage contains a 30-mΩ, 650-V GaN power transistor and specialized driver in an 12-mm × 12-mm QFN package. Direct drive architecture is used to create a normally-off device while providing the native switching performance of the GaN power transistor. When the LMG3522 is unpowered, an integrated low-voltage silicon MOSFET turns the GaN device off through its source. In normal operation, the low-voltage silicon MOSFET is held on continuously while the GaN device is gated directly from an internally-generated negative voltage supply. The integrated driver provides additional protection and convenience features. Fast overcurrent, overtemperature, and undervoltage lockout (UVLO) protections help create a fail-safe system. The device's status is indicated by the FAULT output. An internal 5-V low-dropout regulator can provide up to 5 mA to supply external signal isolators. Finally, externally-adjustable slew rate and a low-inductance QFN package minimize switching loss, drain ringing, and electrical noise generation.

AMC1306

The AMC1306 is a precision, delta-sigma (ΔΣ) modulator with the output separated from the input circuitry by a capacitive double isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced isolation of up to 7000 VPEAK according to the DIN VDE V 0884-11 and UL1577 standards. Used in conjunction with isolated power supplies, this isolated modulator separates parts of the system that operate on different commonmode voltage levels and protects lower-voltage parts from damage.

TMCS1133

The TMCS1133 is a galvanically isolated Hall-effect current sensor with industry leading isolation and accuracy. An output voltage proportional to the input current is provided with excellent linearity and low drift at all sensitivity options. Precision signal conditioning circuitry with built-in drift compensation is capable of less than 2.5% maximum total error over temperature and lifetime with no system level calibration, or less than 1.5% maximum total error with a one-time room temperature calibration (including both lifetime and temperature drift).

UCC2122

The UCC21222 device is an isolated dual channel gate driver with programmable dead time. It is designed with 4A peak-source and 6A peak-sink current to drive power MOSFET, IGBT, and GaN transistors. The device can be configured as two low-side drivers, two high-side drivers, or a half-bridge driver. A 5ns delay matching performance allows two outputs to be paralleled, doubling the drive strength for heavy load conditions without risk of internal shoot-through. The input side is isolated from the two output drivers by a 3.0kVRMS isolation barrier, with a minimum of 100V/ns common-mode transient immunity (CMTI).

UCC27712

The UCC27712 is a 620-V high-side, low-side gate driver with 1.8-A source and 2.8-A sink current capability that is targeted to drive power MOSFETs or IGBTs. The device comprises of one ground-

referenced channel (LO) and one floating channel (HO), which is designed for operating with bootstrap supplies. The device features excellent robustness and noise immunity with capability to maintain operational logic at negative voltages of up to –8 VDC on HS pin (at VDD = 12 V).

2. System Design Theory

2.1 PWM

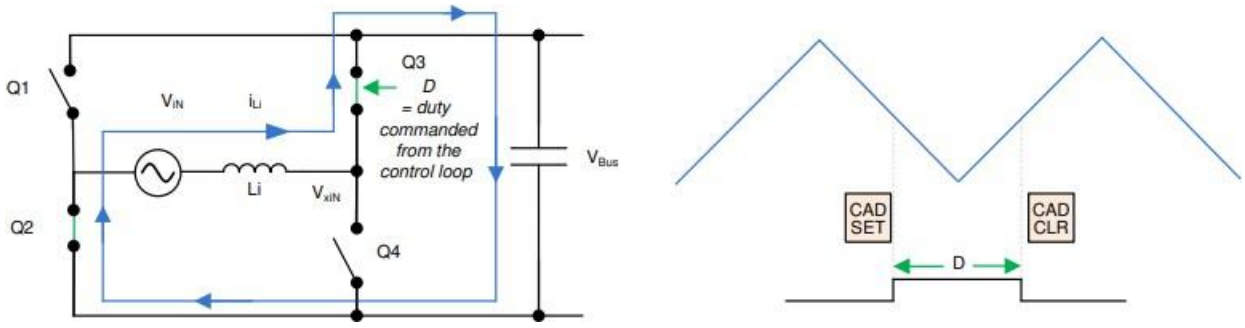


Figure 2.1. Single-Phase Diagram of TTPL PFC.

Figure 2.1 shows a simplified diagram of a single phase of the interleaved TTPL PFC topology. To control this rectifier the duty cycle is controlled to regulate the voltage directly. This regulation is possible if the software variable Duty or D is set so that when it is equal to 1, Q3 is always ON, and the setting makes the voltage VxiN equal to the Vbus voltage. When Duty is set to 0, Q3 never turns on, and Q4 is always connected which makes the VxiN voltage go to 0.

2.2. Current Loop Model

To understand the current loop model, first look at the inductor current closely. In Figure 2.1, the Duty cycle (D) is provided to the PWM modulator, which is connected to the switch Q3 and Q4. From here, Equation 1 is written as:

$$V_{XiN} = D \times V_{bus} \qquad (1)$$

To modulate the current through the inductor, the voltage VxiN is regulated using the duty cycle control of Q3 and Q4 switches. It is assumed that the direction of current is positive in the direction from the AC line into the rectifier and that the grid is fairly stiff when using the DC bus feedforward and the AC voltage feedforward. Figure 2.2 shows the simplified current loop, and the current loop plant model is written as Equation 2

$$H_{P_i} = \frac{i_{Li}^*}{D} = \frac{1}{K_{v_gain}} \times K_{i_gain} \times K_{i_fltr} \times G_d \times \frac{1}{Z_i} \qquad (2)$$

Where:

- K_{v_gain} is the inverse of the maximum bus voltage sensed,
- K_{i_gain} is the inverse of the maximum AC sensed,
- $K_{i_{fltr}}$ is the response of the RC filter connected from the current sensor to the ADC pin
- G_d is the digital delay associated with the PWM update and digital control is the current command
- $i_{Li}^*$is the current command

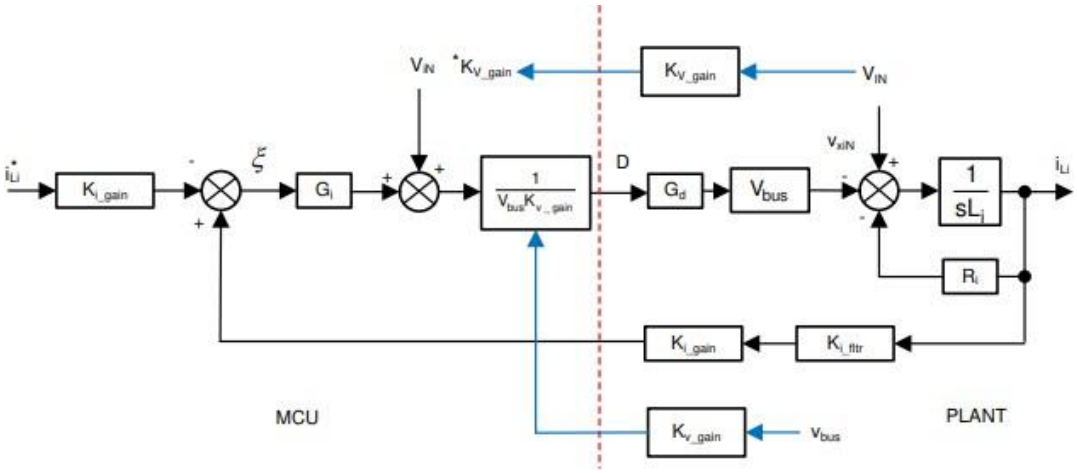


Figure 2.2. Current Loop Control Model.

Note

The negative sign on the reference is because the current loop is thought to be regulating the voltage, VxiN. To increase the current, VxiN must be reduced—hence, the opposite sign for reference and feedback is in Figure 2.2.

This current loop model is then used to design the current compensator. A simple proportional integral controller is used for the current loop.

2.3. DC Bus Regulation Loop

The DC bus regulation loop is assumed to provide the power reference. The power reference is then divided by the square of the line voltages RMS to provide the conductance, which is further multiplied by the line voltage giving the instantaneous current command.

Small signal model of the DC bus regulation loop is developed by linearizing Equation 4 around the operating point.

$$i_{DC}v_{bus} = \eta V_{Nrms} i_{Nrms} \rightarrow \hat{\imath}_{DC} = \eta \frac{V_{Nrms}}{V_{bus}} i_{Li} \qquad (3)$$

For a resistive load the bus voltage and current are related as shown in Equation 5.

$$V_{bus} = \frac{R_L}{1 + sR_L C_o} \hat{\imath}_{DC} \qquad (4)$$

The DC voltage regulation loop control model can be drawn as shown in Figure 2.3. An additional Vbus feedforward is applied to make the control loop independent of the bus voltage, and hence, the plant model for the bus control can be written as Equation 5.

$$H_{p_bus} = H_{load} \times \eta \times K_{i_gain} \times K_{v_gain} \times K_{v_flt} \qquad (5)$$

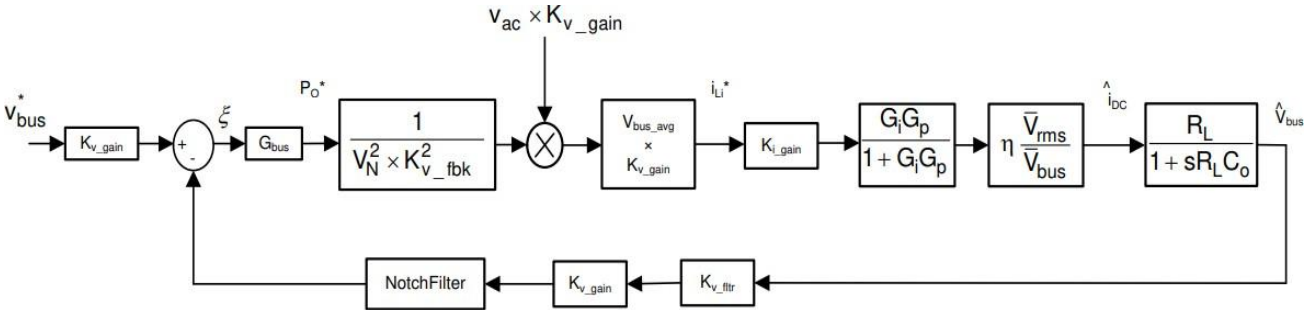


Figure 2.3. DC voltage control loop.

Using Figure 2.3, a proportional integrator (PI) compensator is designed for the voltage loop. The bandwidth of this loop is kept low as it is in conflict with the THD under steady state.

2.4. Soft Start Around Zero Crossing for Eliminate or Reduce Current Spike

Zero crossing current spikes is a challenging issue for TTPL PFC topologies. This issue is solved by implementing a soft start scheme with a state machine to turn on and off switches in a particular sequence.

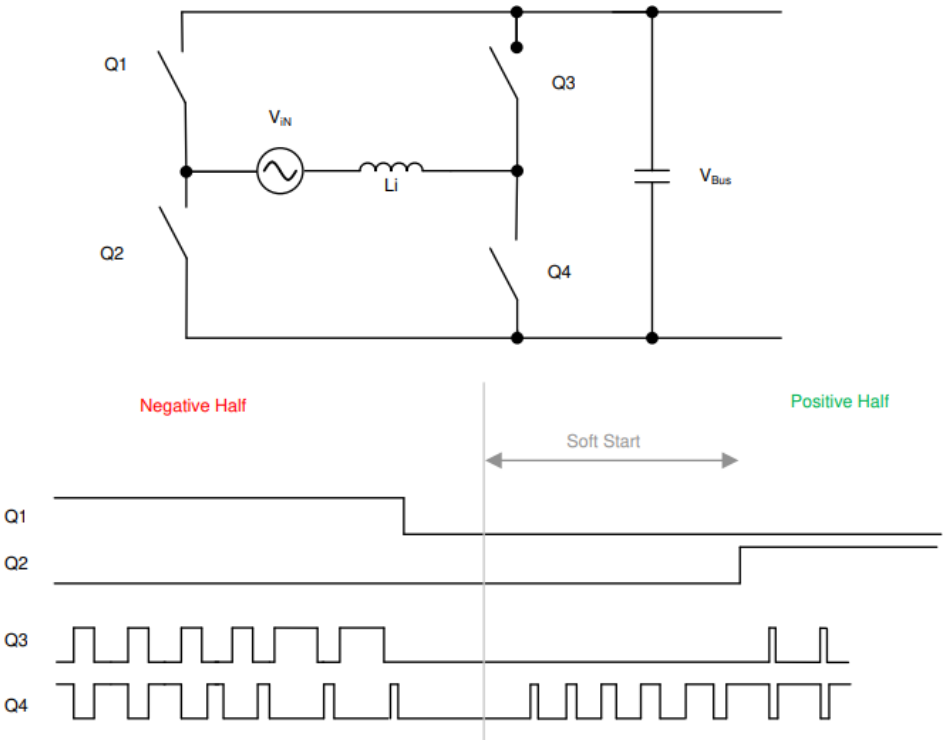


Figure 2.4. PWM Sequence with Soft Starting to Reduce Current Spike at Zero Crossing.

Figure 2.4 shows the switching sequence when the AC wave goes from negative to positive. During the negative half Q1 is ON, Q3 is the active FET, and Q4 is the sync FET. During this time the voltage across Q2 is the DC bus voltage. When the AC cycle changes, Q2 must be at 100% or close to 100%. If Q2 is turned ON immediately, a huge positive spike results. Therefore, a soft-start sequence is used to turn Q4 ON as shown in Figure 2-13. The tuning of this soft start depends on the inductance value and other power stage parameters such

as device Coss. Another reason for a negative current spike around zero crossing is the relatively low AC voltage around the zero crossing. When Q3 is turned ON, though the duty cycle is low, a high-voltage difference is applied and can result in a high negative current spike. Therefore, a sufficient delay is applied before Q3 starts switching back again. Similarly, Q2 is turned on after some delay after the soft start has started.

3. C2000 connection and Hardware Setting

Figure 3.1 shows a high-level view of how signals are interfaced between the main board and the C2000 microcontroller. The key signal connections between the MCU and the power board are listed in the table below. The image of the main board with its components are shown in Figure 3.2.The device memory and the MIPs requirement for this reference design is approximately 40kB and 90 MIPS.

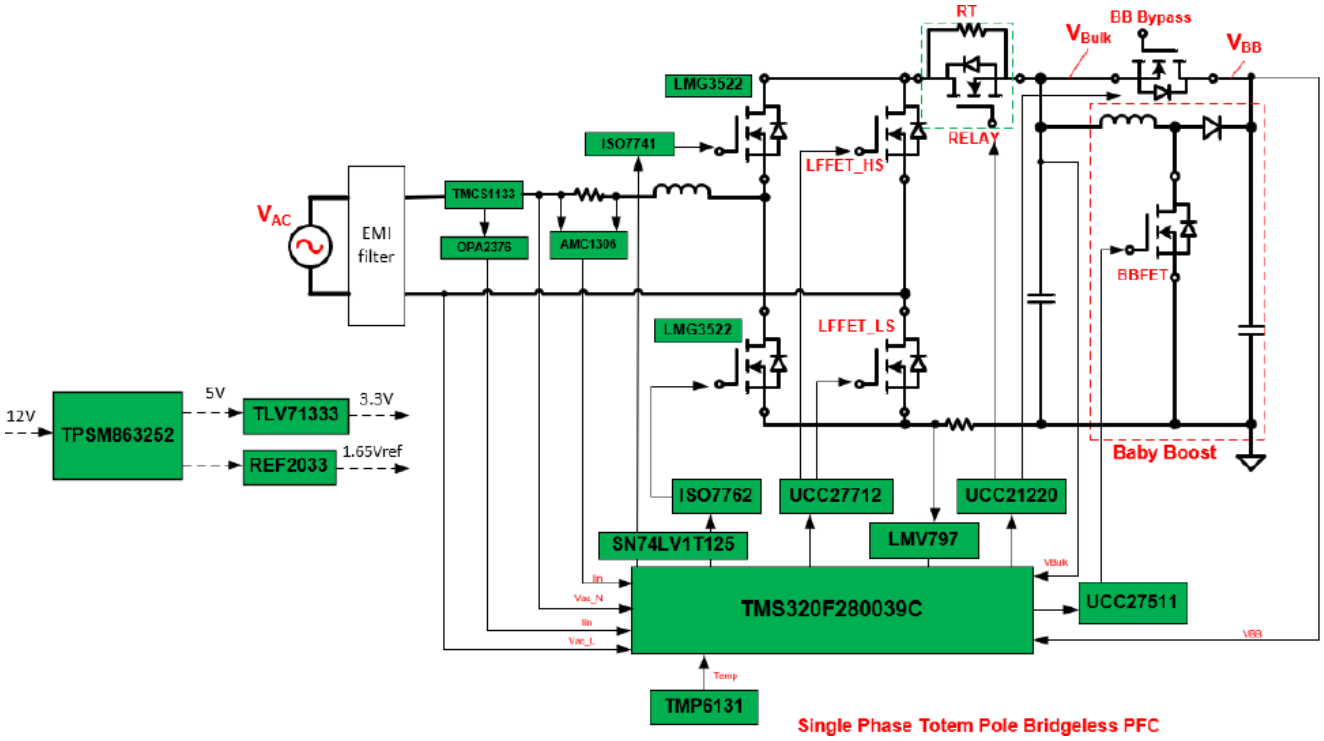


Figure 3.1. Signals interfaced between C2000 MCU and the main board.

Table 4.1. Key signals between the MCU and main board.

Power Stage Signal	Description	F28003x MCU Pin
LFFET_HS	PWM driver for low frequency FET high side	GPIO-00/PWM1A
LFFET_LS	PWM driver for low frequency FET low side	GPIO-01/PWM1B
HFFET_HS	PWM driver for high frequency FET high side	GPIO-02/PWM2A
HFFET_LS	PWM driver for high frequency FET low side	GPIO-03/PWM2B
BBDRV	PWM driver for baby boost	GPIO-06/PWM4A
AC_L	AC line sensed signal	ADC B3
AC_N	AC neutral sensed signal	ADC B8
AC_CUR	AC current sensed signal	ADC C6
VBulk	Bus voltage sensed signal before baby boost	ADC A0
VBB	Bus voltage sensed signal after baby boost	ADC A7
RELAY_CTRL	Inrush relay control signal	GPIO 12
ZCD	Zero current detection	ADC C14
I_inrush	Inrush current sense	ADC C1
SD CLK	Clock soure for SDFM	GPIO15/EPWM8B
SD1_C3	Clock for Filter-3	GPIO21
SD1_D3	Data for Filter-3	GPIO20
SD1_C4	Clock for Filter-4	GPIO23
SD1_D4	Data for Filter-4	GPIO22

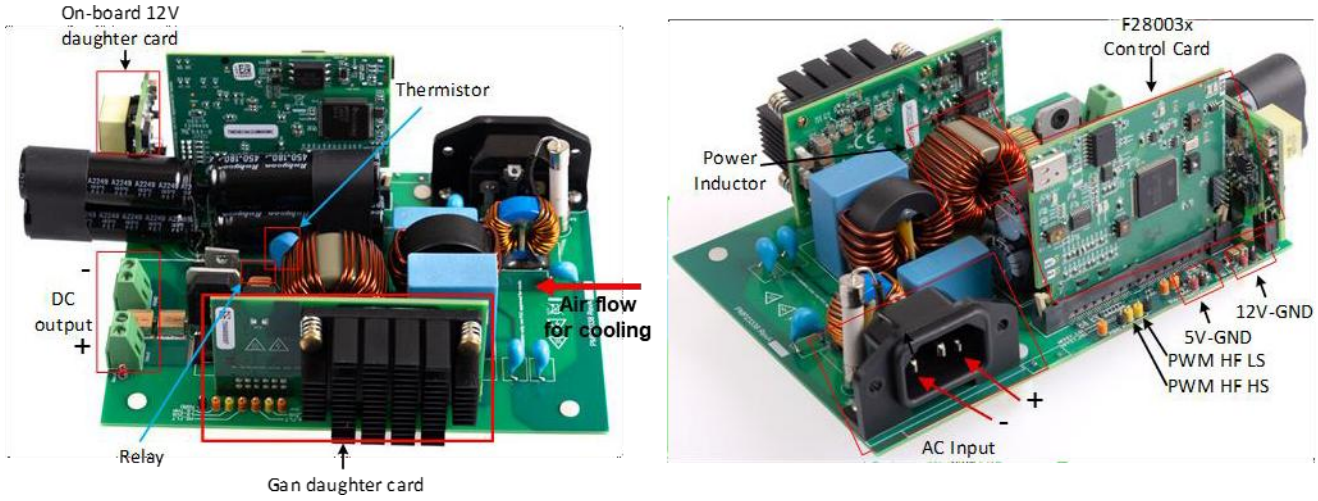
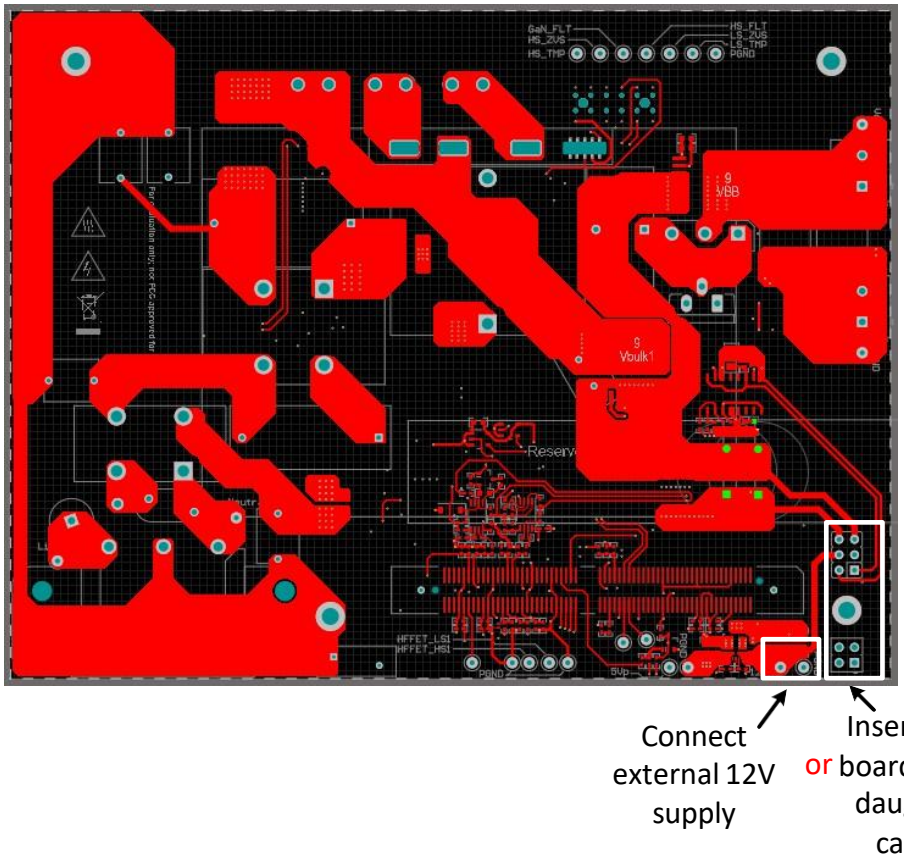


Figure 3.2. PMP 23338 board with its main components.

Important:

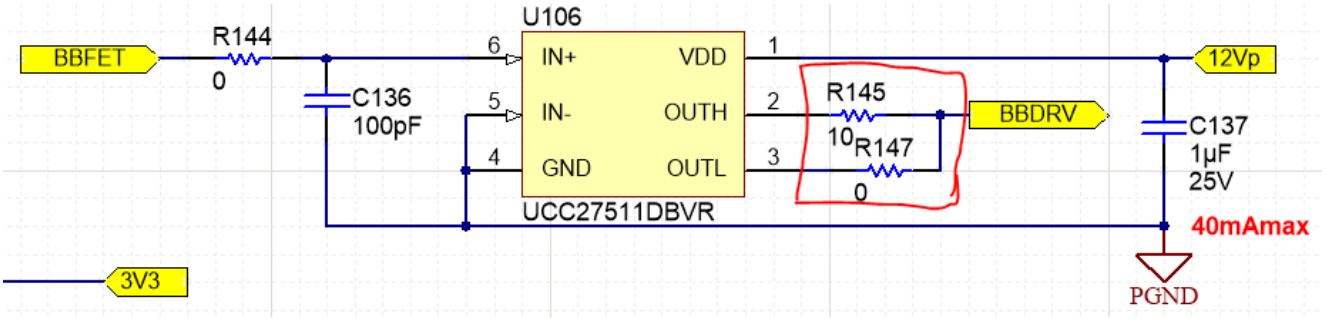
1. **12V supply**: The pmp23338 board has on-board 12V auxiliary power supply daughter card. External 12V biased supply can also be used for preliminary tests. Both of them must **NOT** be used at the same time.



The onboard biased daughter card requires approximately 130V at DC bus voltage to generate 12V. This needs at least 110V AC input. Hence, any experiment that involves less than 130V at the DC bus should be conducted with an external 12V biased supply. Therefore, it is recommended to use the **onboard** 12V daughter card only for Build-4(b). Also, for E-meter functionality, on-board bias must be used. The external 12V supply can be used for all the Builds/labs. Details for running different labs are provided in the next section.

2. **Relay**: When using external 12V bias supply (for preliminary tests), the relay is not operated. Hence, relay **MUST** be shorted which can be done by manually shorting the thermistor RT2 on the back side of the board.

3. **Baby boost**: When using external 12V bias supply (for preliminary tests), baby boost **MUST** be disabled before powering up the board. To disable the baby boost, short the baby boost bypassing FET Q102 on the main board. Also, R145 and R147 **MUST** be removed. Otherwise, the board may get damaged.



4. Software

Note: If you are using DPSDK 6.00 for pmp23338 software, you must use CCS version 21.0.0 and compiler version 25.11.1.LTS.

4.1 Importing the project

1. Download C2000Ware Digital Power SDK, from ti.com and save it to your system. The PMP 23338 project and its supporting files are contained in this folder.
2. Open CCSv12 (or newer). Maximize the program to fill the screen. Close the welcome screen if it opens up.
3. On the menu bar click Project → Import Existing CCS/CCE Eclipse Project. Select root directory, navigate to the downloaded C2000Ware Digital Power SDK folder, and select solutions→pmp23338→/28003x→ccs. Click Finish. This project invokes all the necessary tools (compiler, assembler, linker) to build the project.
4. Save the file and build the project.

4.2. Software Flow Diagram

The software consists of two interrupt service routine (ISR). The voltage controller loop is updated in the 10kHz ISR. The sensed value of voltage and current are updated in the 65kHz ISR. The current controller is implemented in 65kHz ISR.

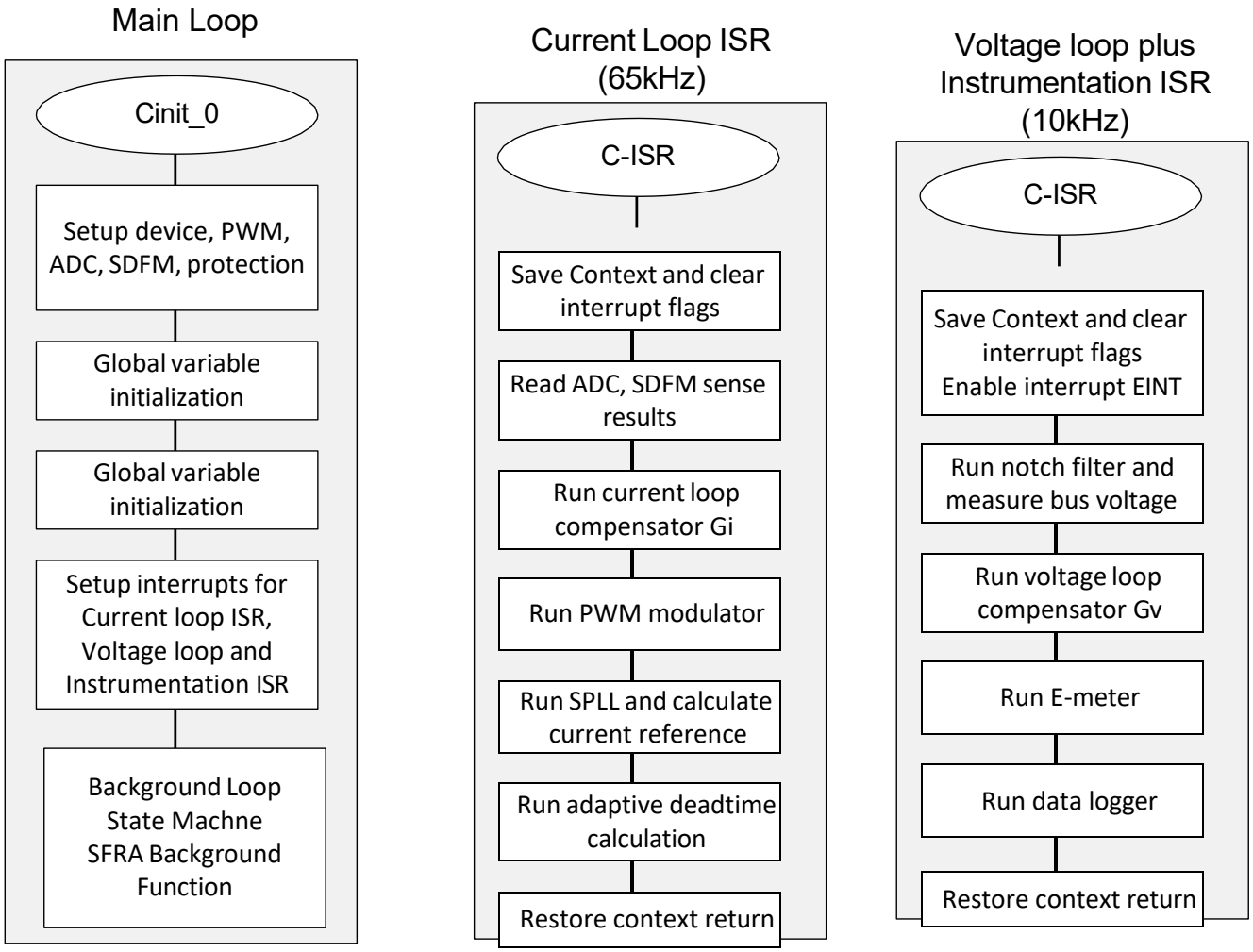


Figure 4.1. Software Flow Diagram.

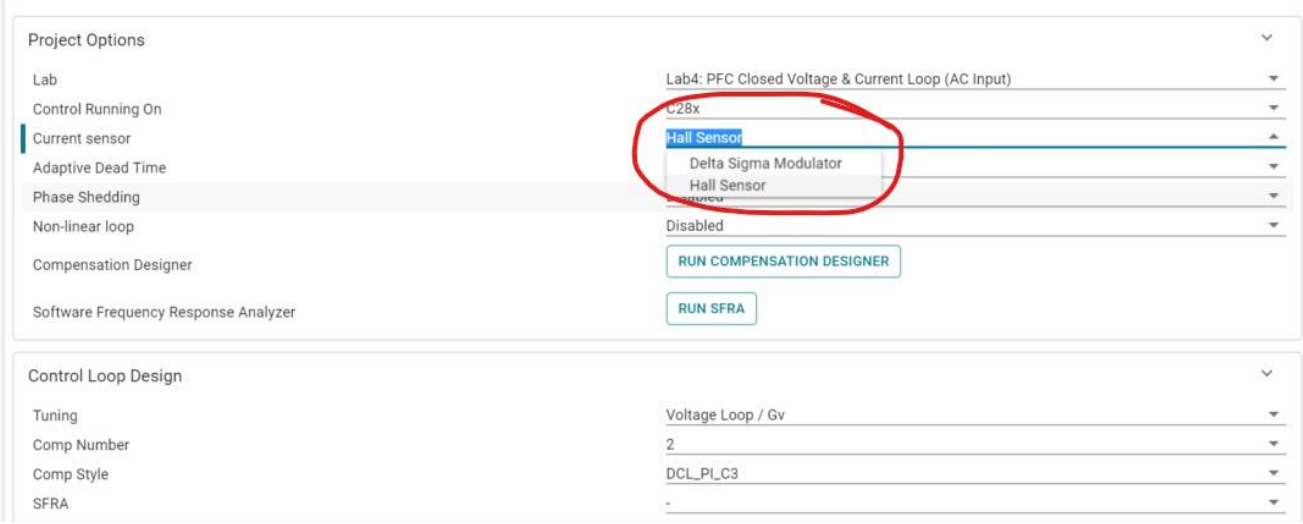
5. Procedure for running the Project

Direct evaluation

The PMP23338 board (PFC23338EVM-107) ordered from ti.com is fully tested. The board does not need any modification. A user can follow section 2 of PFC23338EVM-107 EVM User's guide to flash the code, and section 3 to power up the board using F28003x control card.

Step-by-step evaluation

For step-by-step evaluation, five types of builds/labs are created to test a the PFC board. These are named as Build 1-3, Build 4(a) and Build 4(b). Build-1 to Build-4(a) use the external 12V supply. Therefore, the relay and baby boost bypass FETS **MUST** be shorted, and R145 and R147 **MUST** be removed from the main board. Also, hall sensor must be used for current sensing in Build-1 to Build-4(a). Option for hall sensor can be selected in main.syscfg.



Note that the supply for AMC1306 is given by **on-board** 12V daughter card. So Delta-Sigma based current sensing can **NOT** be used when using an external 12V supply in Builds 1- 4 (a). The purpose and procedure of each build are detailed in the subsequent subsections. The steps for the initial hardware and software are described in the previous sections

5.1. Build 1 : open loop check with DC input

In this lab, the board is excited in open loop fashion with a fixed duty cycle. The duty cycle is controlled with dutyPU_DC variable. This build verifies the sensing of feedback values from the power stage and also operation of the PWM gate driver and ensures there are no hardware issues. Additionally, calibration of input and output voltage sensing can be performed in this build.

5.1.1. Setting the hardware for Build-1

- Make sure no power source is connected to the board.
- Insert the F28003x control card in the slot provided.
- Connect an external 12-V DC power supply. Make sure the relay and baby boost are shorted and, R145 and R147 are removed from the main board if using external 12V auxiliary power supply. Also, the on-board 12V daughter card MUST not be connected when using external 12V.

- Turn the 12-V power supply ON. The LED on the control card lights up and indicates the device is powered.
- To connect JTAG, use a USB cable from the control card and connect it to a host computer.

5.1.2. Setting the software for Build-1

- Make sure the control card is connected to the board as described in the previous sections.
- Turn on the 12V power supply.
- Expand the project and double-click on “main.syscfg” file. The powerSUITE page opens.
- On the powerSUITE page (main.syscfg), scroll down and select Lab-1 under the Lab option. Select “Hall Sensor” for the Current sensing. Also disable the other options such as Non-Linear Voltage Loop, Adaptive Deadtime and Phase shedding
- Under Power Stage Parameters, make sure the switching frequency is 65kHz. Save the page.

5.1.3. Building and Loading Project

- Right-click on the project name, and click Rebuild Project
- Then click Run → Debug. This action launches a debugging session. In the case of dual CPU devices, a window may appear to select the CPU that the debug must be performed. In this case, select CPU1.
- The project then loads on the device, and CCS debug view becomes active. The code halts at the start of the main routine.

5.1.4. Setup Debug Environment Windows

- To add the variables in the watch and expressions window, click View → Scripting Console to open the scripting console dialog box. On the upper-right corner of this console, click on open then browse to the setupdebugenv_lab1.js script file located inside the project folder. This script file populates the watch window with the appropriate variables required to debug the system. Click on the Continuous Refresh button on the watch window to enable continuous update of values from the controller.
- Run the project by clicking on .
- Now Halt the processor by using the Halt button on the toolbar

5.1.5. Running the code

- Connect a DC power supply with rating of 100V, 4 A to input and a resistive load of approximately 200Ω to the output. Make sure to connect the DC input with correct polarity (see Fig. 3.2). Do not turn on the power supply yet. Use a current limit protection of 4A from the DC source for this build.
- Debug the project again. Run the project by clicking on
- In a few seconds, after the variable “autoStartSlew” reaches 100, the trip clears, and a duty cycle of 0.5 is applied. At this point, you can probe the PWM signals.
- In the watch view, check if the TTPLPFC_ac_vol_sensed_Volts, TTPLPFC_vBus_sensed_Volts, TTPLPFC_ac_cur_sensed_Amps, variables are updating, periodically. These values should be around 0 as no input is provided.
- Now slowly increase the input DC voltage from zero to 20 V. The output voltage should show boosted voltage as a steady duty cycle of 0.5 PU is applied as default setting. If everything in the variables looks good in the expression window, you can further increase the input voltage up to 100V. If a high current is drawn, verify if the voltage terminals are swapped. If true, reduce the voltage to zero first and correct the issue before resuming the test.
- Make sure TTPLPFC_ac_vol_sensed_Volts and TTPLPFC_vBus_sensed_Volts display the correct values, for 100-V DC input, TTPLPFC_vBus_sensed_Volts is close to 200V. This verifies the voltage sensing of the board in some manner.
- This verifies at a basic level the PWM driver and connection of hardware, user can change the dutyPU_DC variable to see operation under various boost conditions.
- This completes the check for this build. The controller can now be halted, and the debug connection is terminated. Click to halt the controller then click to terminate the debug session. Reduce the input voltage to 0.

5.2. Build 2 : Closed Current Loop with DC input

In this Build, the inner current loop is closed, that is, the inductor current is controlled using a current compensator Gi. The input voltage feed forward is applied to the output of this current compensator to generate the duty cycle.

5.2.1. Setting the hardware for Build-2

- Make sure no power source is connected to the board.
- Insert the F28003x control card in the slot provided.
- Connect an external 12-V DC power supply. Make sure the relay and baby boost are shorted and, R145 and R147 are removed from the main board if using external 12V auxiliary power supply. Also, the on-board 12V daughter card MUST not be connected when using external 12V.
- Turn the 12-V power supply ON. The LED on the control card lights up and indicates the device is powered.
- To connect JTAG, use a USB cable from the control card and connect it to a host computer.

5.2.2. Setting the software for Build-2

- Make sure the control card is connected to the board as described in the previous sections.
- Turn on the 12V power supply.
- Expand the project and double-click on “main.syscfg” file. The powerSUITE page opens.
- On the powerSUITE page (main.syscfg), select Lab-2 under the Lab option. Select “Hall Sensor” for the Current sensing. Also disable the other options such as Non-Linear Voltage Loop, Adaptive Deadtime, and Phase shedding
- Under Power Stage Parameters, make sure the switching frequency is 65kHz. Save the page.

5.2.3. Building and Loading Project

- Right-click on the project name, and click Rebuild Project
- Then click Run → Debug. This action launches a debugging session. In the case of dual CPU devices, a window may appear to select the CPU that the debug must be performed. In this case, select CPU1.
- The project then loads on the device, and CCS debug view becomes active. The code halts at the start of the main routine.

5.2.4. Setup Debug Environment Windows

- To add the variables in the watch and expressions window, click View → Scripting Console to open the scripting console dialog box. On the upper-right corner of this console, click open then browse to the setupdebugenv_lab2.js script file located inside the project folder. This script file populates the watch window with the appropriate variables required to debug the system. Click on the Continuous Refresh button on the watch window to enable continuous updates of values from the controller.
- Run the project by clicking on .
- Now Halt the processor by using the Halt button on the toolbar

5.2.5. Running the code

- Connect a DC power supply with rating of 100V, 4 A to input and a resistive load of approximately 200Ω to the output. Make sure to connect the DC input with correct polarity (see Fig. 3.2). Do not turn on the power supply yet. Use a current limit protection of 4A from the DC source for this build.
- Debug the project again. Run the project by clicking on
- The project is programmed to drive the inrush relay and clear the trip after a set amount of time, that is, autoStartSlew==100. An input voltage must be applied after hitting run and before this autoslew counter reaches 100. If the counter reaches 100, before voltage is applied at the input, the code must be reset. For which the controller must be brought out of real time mode, a reset performed and restarted.
- Default value of the reference current (TTPLPFC_ac_cur_ref_pu) is 0.03pu.

- Now run the project again by clicking on
- Apply an input voltage of approximately 15 V before the TTPLPFC_autoStartSlew reaches 100. Make sure the current limit on DC source is more than 1.2 A. As soon TTPLPFC_autoStartSlew reaches 100, PWM trip is cleared along with closing the current loop flag.
- The input current regulates around 1.1 A, and the output voltage boosts to approximately 54 V.
- If everything works as expected, you can change the reference current (TTPLPFC_ac_cur_ref_pu) in the steps of 0.01 making sure other parameters are within the limit.
- This completes the check for this build. The controller can now be halted, and the debug connection is terminated. Click to halt the controller then click to terminate the debug session. Reduce the input voltage to 0.

5.3. Build 3: Closed Current loop with AC input

In Lab 3 the inner current loop is closed, that is, the inductor current is controlled using a current compensator Gi. The input voltage feed forward is applied to the output of this current compensator to generate the duty cycle.

5.3.1. Setting the hardware for Build-3

- Make sure no power source is connected to the board.
- Insert the F28003x control card in the slot provided.
- Connect an external 12-V DC power supply. Make sure the relay and baby boost are shorted and, R145 and R147 are removed from the main board if using external 12V auxiliary power supply. Also, the on-board 12V daughter card MUST not be connected when using external 12V.
- Turn the 12-V power supply ON. The LED on the control card lights up and indicates the device is powered.
- To connect JTAG, use a USB cable from the control card and connect it to a host computer.

5.3.2. Setting the software for Build-3

- Make sure the control card is connected to the board as described in the previous sections.
- Turn on the 12V power supply.
- Expand the project and double-click on “main.syscfg” file. The powerSUITE page opens.
- On the powerSUITE page, scroll down and select Lab-3 under the Lab option. Select “Hall Sensor” for the Current sensing.
- The current compensator from the previous build is re-used in this lab so no additional steps are required for tuning the current loop in the lab.

5.3.3. Building and Loading Project

- Right-click on the project name, and click Rebuild Project
- Then click Run → Debug. This action launches a debugging session. In the case of dual CPU devices, a window may appear to select the CPU that the debug must be performed. In this case, select CPU1.
- The project then loads on the device, and CCS debug view becomes active. The code halts at the start of the main routine.

5.3.4. Setup Debug Environment Windows

- To add the variables in the watch and expressions window, click View → Scripting Console to open the scripting console dialog box. On the upper-right corner of this console, click on open then browse to the setupdebugenv_lab3.js script file located inside the project folder. This script file populates the watch window with appropriate variables required to debug the system. Click on the Continuous Refresh button on the watch window to enable continuous updates of values from the controller.

5.3.5. Running the code

- Debug the code again. Do not run the code yet.
- Connect an AC source of 230V, 8A at input and a resistive load of approximately 500Ω to the output. Do not turn on the power supply yet. Use a current limit protection of 8A from the AC source for this build.
- For the first time as a precaution, set the input voltage to 0 and turn on the AC supply. Gradually increase the input voltage to 120V RMS and monitor the current. The output voltage should be close to sqrt(2)*input and the input current should be around 0.5A. This verifies that the board is good. Turn off the AC source.
- The project is programmed to wait for input voltage to exceed approximately 75Vrms to drive the in-rush relay, and clear the trip.
- Now run the code and apply an input voltage of approximately 90 V, the board comes out of the undervoltage condition and inrush relay is driven. The trip clears, and a small amount of current of approximately 0.8-A RMS is drawn. The bus voltage is close to 180 V.
- If everything works as expected, you can change the reference current (TTPLPFC_ac_cur_ref_pu) in the steps of 0.01 making sure other parameters are within the limit.

- This completes the check for this build. The controller can now be halted, and the debug connection is terminated. Click to halt the controller then click to terminate the debug session. Reduce the input voltage to 0 and disconnect the power supply.

5.4. Build 4(a) : Closed Current and Voltage Loop

In this lab the outer voltage loop is closed with the inner current loop closed. A PI-based compensator is used and tuned through the compensation designer for the outer voltage loop.

5.4.1. Setting the hardware for Build-4

- Make sure no power source is connected to the board.
- Insert the F28003x control card in the slot provided.
- Connect an external 12-V DC power supply. Make sure the relay and baby boost are shorted and, R145 and R147 are removed from the main board if using external 12V auxiliary power supply. Also, the on-board 12V daughter card MUST not be connected when using external 12V.
- Turn the 12-V power supply ON. The LED on the control card lights up and indicates the device is powered.
- To connect JTAG, use a USB cable from the control card and connect it to a host computer.

5.4.2. Setting the software for Build-4(a)

- Make sure the control card is connected to the board as described in the previous sections.
- Turn on the 12V power supply.
- Expand the project and double click on “main.syscfg” file. The powerSUITE page opens.
- On the powerSUITE page, scroll down and select Lab-4 under the Lab option. Select “Hall Sensor” for the Current sensing. You can enable Non-Linear Voltage Loop for this build. Disable the other options such as Adaptive Deadtime and Phase shedding.
- Under Power Stage Parameters specify the switching frequency, the dead band, and the power rating. Save the page.
- Under Power Stage Parameters, make sure the switching frequency is 65kHz. Save the page.

5.4.3. Building and Loading Project

- Right click on the project name, and click Rebuild Project
- Then click Run → Debug. This action launches a debugging session. In the case of dual CPU devices, a window may appear to select the CPU that the debug must be performed. In this case, select CPU1.
- The project then loads on the device, and CCS debug view becomes active. The code halts at the start of the main routine

5.4.4. Setup Debug Environment Windows

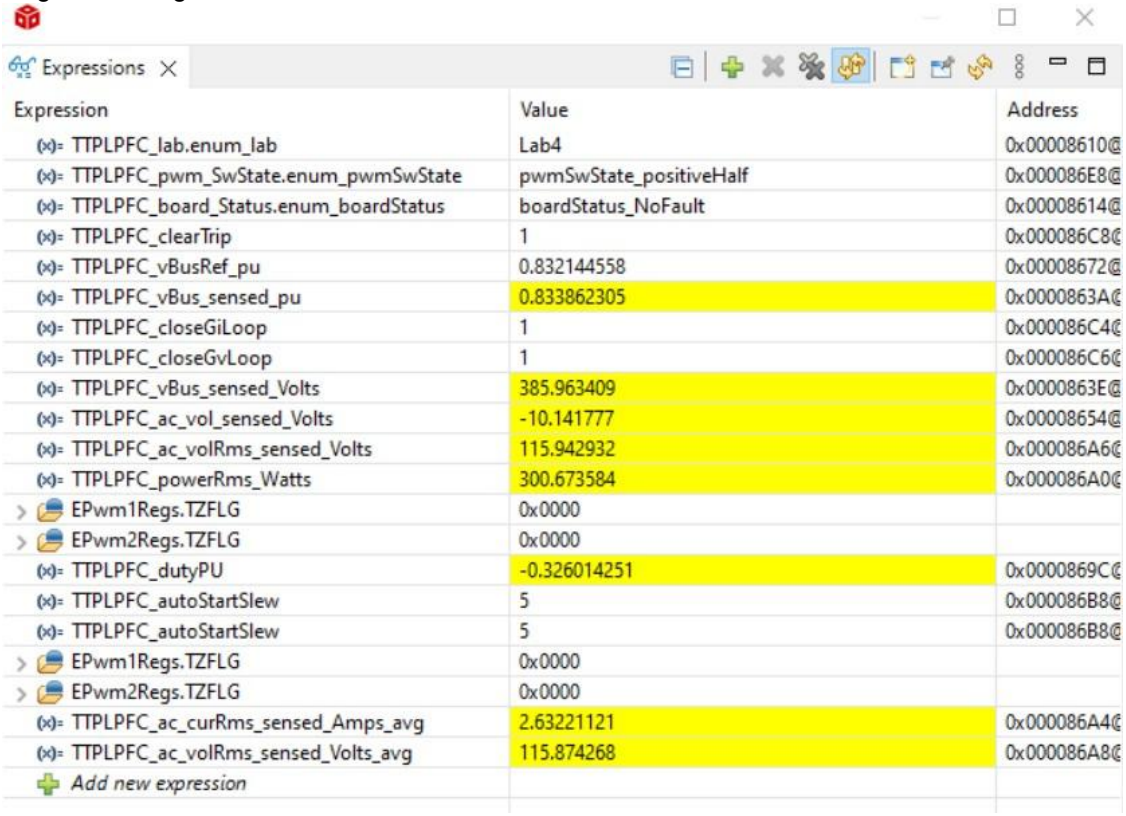
- To add the variables in the watch and expressions window, click View → Scripting Console to open the scripting console dialog box. On the upper-right corner of this console, click on open then browse to the setupdebugenv_lab4.js script file located inside the project folder. This script file populates the watch window with appropriate variables required to debug the system. Click on the Continuous Refresh button on the watch window to enable continuous updates of values from the controller.
- Run the project by clicking on .
- Now Halt the processor by using the Halt button on the toolbar

5.4.5. Running the code

- Debug the code again. Do not run the code yet.
- Connect an AC source of 230V, 8A at input and a resistive load of approximately 500Ω to the output. Do not turn on the power supply yet. Use a current limit protection of 8A from the AC source for this build.
- For the first time as a precaution, set the input voltage to 0 and turn on the AC supply. Gradually increase the input voltage to 120V RMS and monitor the current. The output voltage should be close to sqrt(2)*input

and the input current should be around 0.5A. This verifies that the board is good. Turn off the AC source.

- The project is programmed to wait for input voltage to excel at approximately 75 Vrms to drive the in rush relay, and clear the trip.
- Now run the code and apply an input voltage of approximately 115 V. The board comes out of the undervoltage condition and inrush relay is driven. The trip clears, and the output rises to 385-V DC. A sinusoidal current is drawn from the AC input. Figure 3-28 shows the watch window when the program is running at this stage.



- This completes the check for this build. The controller can now be halted, and the debug connection is terminated. Click to halt the controller then click to terminate the debug session. Reduce the input voltage to 0 and disconnect the power supply.

5.5. Build 4(b): E-meter Test

5.5.1. Hardware Change:

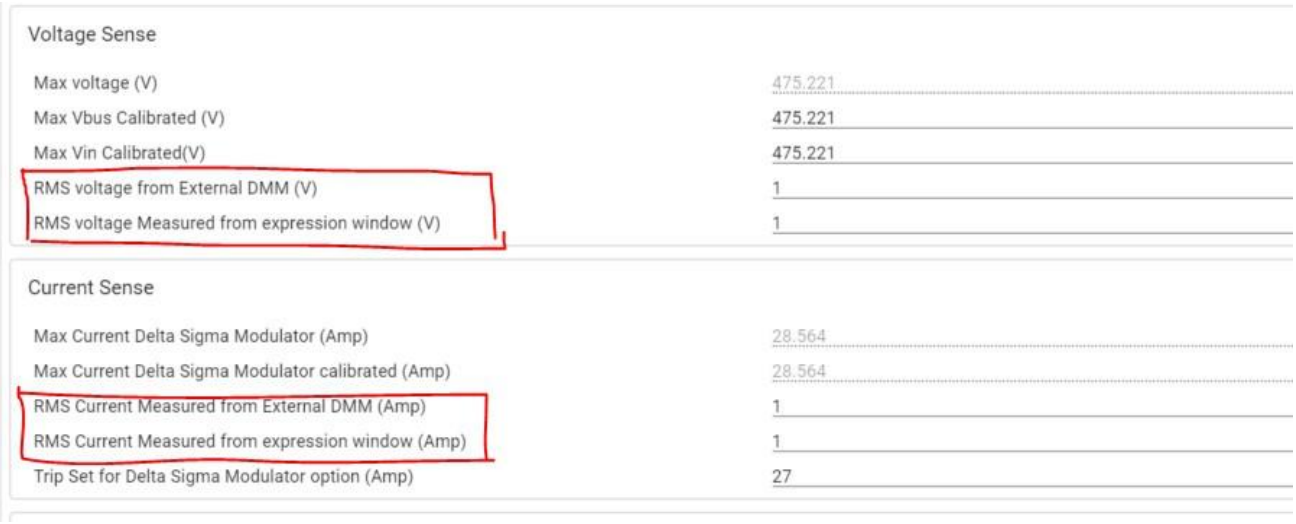
- **Unshort the relay**
- **Unshort the baby boost bypass**
- **Populate , R145 and R147.**
- **Insert the on-board 12V daughter card**
- **Do not use external 12V supply.**

5.5.2. Running Build-4(a) using on-board 12V bias.

- Make sure the control card is connected to the board.
- Make sure the external 12V is **NOT** connected.
- Expand the project and double-click on “main.syscfg” file. The powerSUITE page opens.
- On the powerSUITE page, scroll down and select Lab-4 under the Lab option. Select “Delta Sigma Modulator” for the Current sensing. You can enable Non-Linear Voltage Loop for this build. Disable the other options such as Adaptive Deadtime and Phase shedding.
- Under Power Stage Parameters, make sure the switching frequency is 65kHz. Save the page.
- Connect a 230V, 8A AC source.
- Use and electronic load for this lab and set it in CC mode with 0.1A current. If electronic load is not available, use a variable resistive load (2000Ω-100Ω) and set the initial resistance such that it draws 0.1A output current at 115V AC input.
- Debug the code. **Do not run yet.**
- Turn on the AC supply with 115V RMS. The output voltage should be slightly less than sqrt(2)*input voltage. The reason is that the relay is not shorted now, the current flows through the thermistor which drops a certain amount of voltage across it.
- The on-board 12V daughter card needs at least 130V DC bus voltage. The on-board 12V supply should be working now. (To verify, measure the voltage across 12V-GND).
- Wait for 5 sec after turning on the AC input. After that, run the code. The output voltage should be close to 385V now.

5.5.3. Calibration for E-meter test

- Connect an external meter for measuring input voltage, input current and input power.
- Follow the steps in 6.5.2 to run the code.
- Increase the load to half of the maximum load: 800W. **Note that a fan must be used for cooling.**
- Now note down reading of input current and input voltage from external meter. Similarly note the reading of TTPLPFC_ac_volRms_sensed_Volts_avg and TTPLPFC_ac_curRms_sensed_Amps_avg from the expression window.
- Now switch off the AC supply and stop the code.
- Open the syscfg file and scroll down to “Voltage Sense” and “Current Sense” sections. Enter the values of RMS currents and RMS voltages noted from external meter and expression window. The default values are 1.



- After entering the values, you will observe that “Max Vbus Calibrated (V)” and “Max Current Delta Sigma Modulator calibrated (Amp)” will be modified.
- Now build the code. Open ttplpfc_setting.h and verify that “TTPLPFC_VDCBUS_MAX_SENSE” and “TTPLPFC_VAC_MAX_SENSE” are also modified. Similarly, verify that “TTPLPFC_SD_I_MAX_SENSE” is modified.
- Follow the steps in 5.5.2 again to run the code.
- Now you can compare the input voltage, input current and input power from external meter and the ones in the expression window. The variable for input power in the expression window is **TTPLPFC_powerRms_Watts**.

5.6. Build 5-9.

- Build 5-9 belongs to inverter mode operation. The code of the inverter mode of PMP23338 is being developed and will be provided in subsequent SDK release.

6. Test Results

Please refer to the test report for the efficiency, power factor, THD, E-meter and AC drop performance.